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PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel Mulligan
Serial No: 10/723,169
Filing Date: 11/26/2003
Examiner: Chang, Daniel D
Art Group: 2819
Docket No: SIG000114
Title: PROGRAMMABLE DRIVER FOR USE IN A MULTIPLE FUNCTION HANDHELD DEVICE

Date: 4/17/06

Honorable Commissioner of
Patents and Trademarks,
Alexandria, Virginia 22313

APPELANT'S BRIEF

1. On February 16, 2006, the applicant filed a Notice of Appeal and a Pre-Appeal Brief Request for Review. A Notice of Panel Decision from Pre-Appeal Brief Review was mailed on March 21, 2006. Accordingly, the present Appellant's brief is being filed prior to April 21, 2006.

2. The Commissioner is hereby authorized to charge the fee for filing this Appellant's Brief of $500.00 pursuant to 37 CFR 41.20(b)(2) to SigmaTel Inc. deposit account 50-1415. The Commissioner is further authorized to charge any additional fees, or post any credits, regarding the filing of this Appellant's Brief s to the same deposit account 50-1415.

CERTIFICATE OF MAILING
37 C.F.R 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Alexandria, Virginia 22313, on the date below:

4-17-06 — Diane Hudson
Date — Signature

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3. Real Party in Interest:

The inventors, Daniel Mulligan, Matthew B. Henson, and Fujio Takeda, all of Austin, Texas, have assigned the entire rights, title and interest in and to the invention of the present patent application to SigmaTel, Inc.

4. Related Appeals and Interferences:

The appellant, the Assignee, and the undersigned are not aware of any related Appeals, Interferences, or judicial proceedings that would affect or have a bearing on the Board's decision in the pending appeal.

5. Status of Claims:

The present patent application includes claims 1 – 24 all of which currently stand rejected. The appellant is requesting the Board of Appeals to review the rejection of all 24 claims.

6. Status of Amendments:

There have been no amendments filed subsequent to the close of prosecution.

7. Summary of the Claimed Subject Matter:

Claim 1 claims a programmable driver that includes a first driver, a second driver, and a controller. (Refer to Figure 3 of the present patent application for an embodiment of a programmable driver.) The second driver is operably coupled in parallel with the first driver to drive a signal on to a line at a first drive level when a drive control signal is in a first state. The second driver is in a high-impedance when the drive control signal is in a second state. In the second state, the first driver drives the signal on to the line at a second drive level, wherein the first drive level (i.e., drive provided by the first and second drivers in parallel) is greater than the second drive level (i.e., drive provided by the first driver). The controller is operably coupled to generate the drive control signal based on load requirements of the line.

Claim 7 claims a programmable driver that includes a plurality of tri-state drivers and a controller. (Refer to Figures 3-5 of the present patent application for embodiments of a programmable driver.) The controller is operably coupled to the plurality of tri-state drivers, wherein, based on a line drive requirement, the controller generates a drive control signal that activates at least one of the plurality of tri-state drivers to drive a signal on to a line at a drive level corresponding to the line drive requirement.

Claim 13 claims a multiple function system on a chip integrated circuit that includes a plurality of interface modules, a digital to analog converter, a processing module, on-chip memory, and a programmable driver. (Refer to Figures 1-3 of the present patent application for embodiments of a programmable driver.) The plurality of interface modules is operably coupled to receive digital data from a corresponding plurality of external sources. The digital to analog converter is operably coupled to convert digital signals into analog signals. The on-chip memory is operably coupled to the processing module and at least temporarily stores operational instructions that cause the processing module to produce the digital signals from the digital data.

The programmable driver includes a first driver, a second driver, and a controller. The second driver is operably coupled in parallel with the first driver to drive the analog signals on to a line at a first drive level when a drive control signal is in a first state. The second driver is in a high-impedance state when the drive control signal is in a second state such that the first driver drives the analog signals on to the line at a second drive level, wherein the first drive level is greater than the second drive level. The controller is operably coupled to generate the drive control signal based on load requirements of the line.

Claim 19 claims a multiple function system on a chip integrated circuit that includes a plurality of interface modules, a digital to analog converter, a processing module, on-chip memory, and a programmable driver. (Refer to Figures 1-5 of the present patent application for embodiments of a programmable driver.) The plurality of interface modules is operably coupled to receive digital data from a corresponding

plurality of external sources. The digital to analog converter is operably coupled to convert digital signals into analog signals. The on-chip memory is operably coupled to the processing module and at least temporarily stores operational instructions that cause the processing module to produce the digital signals from the digital data.

The programmable driver includes a plurality of tri-state drivers and a controller. The controller is operably coupled to the plurality of tri-state drivers and, based on a line drive requirement, generates a drive control signal that activates at least one of the plurality of tri-state drivers to drive the analog signals on to a line at a drive level corresponding to the line drive requirement.

8. Issues to be Reviewed on Appeal:

A. Claims 1-12 have been rejected under 35 USC § 102 (b) as being anticipated by McMahan (U.S. Patent No. 5,859,541).

B. Claims 13-24 have been rejected under 35 USC § 103 (a) as being unpatentable over McMahan (U.S. Patent No. 5,859,541) in view of Pruett (U.S. Patent No. 6,490,121).

9. Argument:

A. Claims 1-12 have been rejected under 35 USC § 102 (b) as being anticipated by McMahan (U.S. Patent No. 5,859,541). All of these claims will be argued as a group.

Claims 1-12 were rejected as anticipated by McMahan. In making the rejection, the Examiner reads the output buffers 42, 44 and 46 on the first, second and third drivers of Applicant's invention. McMahan's output buffers each have a single corresponding impedance. For instance, output buffer 42 has an impedance Z_1, output buffer 44 has an impedance Z_2, etc. The output impedance is controlled by connecting or disconnecting each of the output buffer stages.

Claim 1 recites a programmable driver in accordance with an embodiment of Applicant's invention. This embodiment includes a first driver, and a second driver that is operably coupled in parallel with the first driver to drive a signal on to a line at a first drive level when a drive control signal is in a first state and wherein, when the drive control signal is in a second state, the second driver is in a high-impedance state, such that the first driver drives the signal on to the line at a second drive level, wherein the first drive level is greater than the second drive level. McMahan does not disclose such a second driver. McMahan's output buffers are either connected, providing a predetermined impedance, or disconnected, so as to control the overall output impedance. McMahan does not disclose suggest or teach a configuration where the drive level is controlled in a first and second state between first and second drive levels. Further, McMahan does not disclose suggest or teach placing a second driver in a high-impedance state. Applicant thus believes that claim 1 and claims 2-6 that depend therefrom, are patentably distinct from the prior art.

In the final office action of 8/23/05, the Examiner maintained the rejection and rationale therefore from the office action of 3/21/05 and has provided a response to the applicant's argument. In particular, the Examiner's response to arguments focuses on McMahan teaching that the output buffer may be tri-stated based on the various quotes

regarding the states of the control signals. McMahan does not teach that the various buffers may be tri-stated (e.g., on, off, or in a high impedance state), but teaches that they the buffers are either connected via a coupling transistor to the output pin or not. (Column 4, lines 39-43) Thus, McMahan does not teach or suggest a second driver as is claimed in claim 1.

In addition, the Examiner has apparently overlooked the other arguments of the applicant. In particular, with respect to claim 1, the applicant made the argument that:

> McMahan's output buffers are either connected, providing a predetermined impedance, or disconnected, so as to control the overall output impedance. McMahan does not disclose suggest or teach a configuration where the drive level is controlled in a first and second state between first and second drive levels [based on the load requirements of the line being driven by the programmable driver].

The applicant contends that controlling the output impedance of an output buffer as taught by McMahan is not the equivalent of, or suggestive of, controlling the driver level (e.g., the power level capabilities) of the programmable driver of the present invention. For instance, a buffer may have a desired output impedance but fail to provide the necessary drive if the load of the buffer is too great. McMahan does not address, teach, or suggest generating a control signal based on the load requirements of the programmable driver as is presently claimed in claim 1, but teaches generating control signals based on a desired output impedance.

In particular, McMahan teaches, at column 4 lines 8-13, [a] high-performance application using a terminated line requires a low output impedance in order to obtain proper logic levels at the output. A lower cost, non-terminated line application requires a higher impedance to avoid unacceptable line ringing. The embodiments of Figures 3 and 4 provide an output buffer having a selectable output impedance.

Clearly, adjusting the output impedance of a buffer to accommodate for different line terminations of McMahan is not the equivalent of, or suggestive of, adjusting the

drive capabilities of a programmable driver to accommodate for load requirements of claim 1. Therefore, claim 1-12 are not anticipated by McMahan.

B. Claims 13-24 have been rejected under 35 USC § 103 (a) as being unpatentable over McMahan (U.S. Patent No. 5,859,541) in view of Pruett (U.S. Patent No. 6,490,121). All of these claims will be argued as a group.

Claim 13 recites a multiple function system on a chip integrated circuit in accordance with an embodiment of Applicant's invention. Like claim 1, this embodiment also includes a second driver that is operably coupled in parallel with the first driver to drive a signal on to a line at a first drive level when a drive control signal is in a first state and wherein, when the drive control signal is in a second state, the second driver is in a high-impedance state, such that the first driver drives the signal on to the line at a second drive level, wherein the first drive level is greater than the second drive level. As set forth above, McMahan does not disclose suggest or teach a configuration where the drive level is controlled in a first and second state between first and second drive levels. Applicant thus believes that claim 13 and claims 14-18 that depend therefrom, are patentably distinct from the prior art.

Claim 19 recites a multiple function system on a chip integrated circuit in accordance with an embodiment of Applicant's invention. Like claim 7, this embodiment also includes a plurality of tri-state drivers. As set forth above, McMahan does not disclose tri-state drivers. Applicant thus believes that claim 19 and claims 20-24 that depend therefrom, are patentably distinct from the prior art.

Therefore, claim 13-24 are not obvious in view of McMahan.

Based on the foregoing arguments, the applicant respectfully requests that the Board of Appeals pass claims 1-24 to allowance.

RESPECTFULLY SUBMITTED,

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Claim Appendix:

1. (Original) A programmable driver comprises:

a first driver;

a second driver operably coupled in parallel with the first driver to drive a signal on to a line at a first drive level when a drive control signal is in a first state and wherein, when the drive control signal is in a second state, the second driver is in a high-impedance state such that the first driver drives the signal on to the line at a second drive level, wherein the first drive level is greater than the second drive level; and

controller operably coupled to generate the drive control signal based on load requirements of the line.

2. (Original) The programmable driver of claim 1, wherein the first driver further comprises a tri-state driver that is placed in a high impedance state when an output enable signal is in a first state and is placed in an active state when the output enable signal is in a second state.

3. (Original) The programmable driver of claim 2, wherein the controller further functions to generate the drive control signal in the second state when the output enable signal is in the first state.

4. (Original) The programmable driver of claim 1 further comprises:

a third driver operably coupled in parallel with the first driver to drive the signal on to the line at a third drive level when the drive control signal is in a third state and wherein, when the drive control signal is in the second state, the third driver is in the high-impedance state, wherein the third drive level is greater than the second drive level.

5. (Original) The programmable driver of claim 4, wherein the controller further functions to:

generate the drive control signal in a fourth state, wherein, with the drive control signal in the fourth state, the first, second, and third drivers are coupled on parallel to drive the signal on to the line at a fourth drive level, wherein the fourth drive level is greater than the third.

6. (Original) The programmable driver of claim 1, wherein the controller further functions to determine the load requirement based on a load impedance on the line or an output signal strength setting.

7. (Original) A programmable driver comprises:

a plurality of tri-state drivers; and

controller operably coupled to the plurality of tri-state drivers, wherein, based on a line drive requirement, the controller generates a drive control signal that activates at least one of the plurality of tri-state drivers to drive a signal on to a line at a drive level corresponding to the line drive requirement.

8. (Original) The programmable driver of claim 7, wherein each of the plurality of tri-state drivers, when in an active mode, provides an individual drive level.

9. (Original) The programmable driver of claim 8, wherein the controller further functions to generate the drive control signal by:

determining a desired drive level based on the line drive requirement;

identifying the at least one of the plurality of tri-state drivers based on the desired drive level and the individual drive levels of each of the plurality of tri-state drivers; and

generating the drive control signal to active the at least one of the plurality of tri-state drivers.

10. (Original) The programmable driver of claim 7, wherein the controller comprises a state machine to generate the drive control signal based on the line drive requirement.

11. (Original) The programmable driver of claim 7, wherein the controller further functions to generate the drive control signal to place the plurality of tri-state drivers in a high impedance state when an output enable signal is in a first state.

12. (Original) The programmable driver of claim 7, wherein the controller further functions to determine the line drive requirement based on a load impedance on the line or an output signal strength setting.

13. (Original) A multiple function system on a chip integrated circuit comprises:

a plurality of interface modules operably coupled to receive digital data from a corresponding plurality of external sources;

a digital to analog converter operably coupled to convert digital signals into analog signals;

a processing module;

on-chip memory operably coupled to the processing module, wherein the on-chip memory at least temporarily stores operational instructions that cause the processing module to produce the digital signals from the digital data; and

programmable driver that includes:

a first driver;

a second driver operably coupled in parallel with the first driver to drive the analog signals on to a line at a first drive level when a drive control signal is in a first state and wherein, when the drive control signal is in a second state, the second driver is in a high-impedance state such that the first driver drives the analog signals on to the line at a second drive level, wherein the first drive level is greater than the second drive level; and

controller operably coupled to generate the drive control signal based on load requirements of the line.

14. (Original) The multiple function system on a chip integrated circuit of claim 13, wherein the first driver further comprises a tri-state driver that is placed in a high impedance state when an output enable signal is in a first state and is placed in an active state when the output enable signal is in a second state.

15. (Original) The multiple function system on a chip integrated circuit of claim 14, wherein the controller further functions to generate the drive control signal in the second state when the output enable signal is in the first state.

16. (Original) The multiple function system on a chip integrated circuit of claim 13, wherein the programmable driver further comprises:

a third driver operably coupled in parallel with the first driver to drive the analog signals on to the line at a third drive level when the drive control signal is in a third state and wherein, when the drive control signal is in the second state, the third driver is in the high-impedance state, wherein the third drive level is greater than the second drive level.

17. (Original) The multiple function system on a chip integrated circuit of claim 16, wherein the controller further functions to:

generate the drive control signal in a fourth state, wherein, with the drive control signal in the fourth state, the first, second, and third drivers are coupled on parallel to drive the analog signals on to the line at a fourth drive level, wherein the fourth drive level is greater than the third.

18. (Original) The multiple function system on a chip integrated circuit of claim 13, wherein the controller further functions to determine the load requirement based on a load impedance on the line or an output signal strength setting.

19. (previously amended) A multiple function system on a chip integrated circuit comprises:

a plurality of interface modules operably coupled to receive digital data from a corresponding plurality of external sources;

a digital to analog converter operably coupled to convert digital signals into analog signals;

a processing module;

on-chip memory operably coupled to the processing module, wherein the on-chip memory at least temporarily stores operational instructions that cause the processing module to produce the digital signals from the digital data; and

programmable driver that includes:

a plurality of tri-state drivers; and

controller operably coupled to the plurality of tri-state drivers, wherein, based on a line drive requirement, the controller generates a drive control signal that

activates at least one of the plurality of tri-state drivers to drive the analog signals on to a line at a drive level corresponding to the line drive requirement.

20. (Original) The multiple function system on a chip integrated circuit of claim 19, wherein each of the plurality of tri-state drivers, when in an active mode, provides an individual drive level.

21. (Original) The multiple function system on a chip integrated circuit of claim 20, wherein the controller further functions to generate the drive control signal by:

determining a desired drive level based on the line drive requirement;

identifying the at least one of the plurality of tri-state drivers based on the desired drive level and the individual drive levels of each of the plurality of tri-state drivers; and

generating the drive control signal to active the at least one of the plurality of tri-state drivers.

22. (Original) The multiple function system on a chip integrated circuit of claim 19, wherein the controller comprises a state machine to generate the drive control signal based on the line drive requirement.

23. (Original) The multiple function system on a chip integrated circuit of claim 19, wherein the controller further functions to generate the drive control signal to place the plurality of tri-state drivers in a high impedance state when an output enable signal is in a first state.

24. (Original) The multiple function system on a chip integrated circuit of claim 19, wherein the controller further functions to determine the line drive requirement based on a load impedance on the line or an output signal strength setting.